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Design criteria for an uninterruptable power source (UPS)

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Abstract

This paper on uninterruptible power source (UPS) is a result of an R&D project; it describes the components of a UPS system and reviews the design requirements necessary for its construction with low cost and ease of maintenance.

Keywords: Design criteria; Uninterruptable power sources

1. Introduction

With the proliferation of personal computer systems, there is a growing need for power supply subunits especially for those environments where power supply is generally erratic. Power supply backups are particularly necessary in case of a sudden power failure.

A stand-by generator with an automatic power failure unit which can start the gen-set within seconds of power failure may be used; it switches off when the power supply has been restored. To support each available PC with a generator set would be prohibitively expensive. Commercially available uninterruptable power sources (UPS) variants exist equipped with several internally rechargeable small dry cell units (batteries). Each of such a UPS unit is at half price of a PC. The R&D efforts aim at producing a low-cost maintenance-free version. It consists mainly of a 12 V battery with a charger unit which charges the battery when the power is 'on'. There is also an inverter unit which generates the required a.c. supply from the battery when the power supply fails. A control unit which effects the transition when the power fails and when it is restored.

2. Circuit design

The UPS consists of the following circuits: (i) a thyristor inverter (d.c.–a.c.) incorporating trigger circuits, and (ii) a battery charging circuits.

2.1. D.c.–a.c. thyristor inverter

The basic circuit is as shown in Fig. 1 [1–3].

For a thyristor to conduct it must be forward biased on the application of a sufficient positive signal to the gate: the device will conduct.

When the thyristor Th_1 is conducting, the current will flow from the supply through the inductor, through Th_1 and the winding N_1 and back to the supply. If one assumes that the voltage drops across the choke and the thyristor are negligible, then the capacitor voltage is $2V_{a.c.} = V_c$. When the trigger signal is applied to the gate of the thyristor Th_2, it is switched 'on' and the capacitor voltage V_c appears across thyristor Th_1.

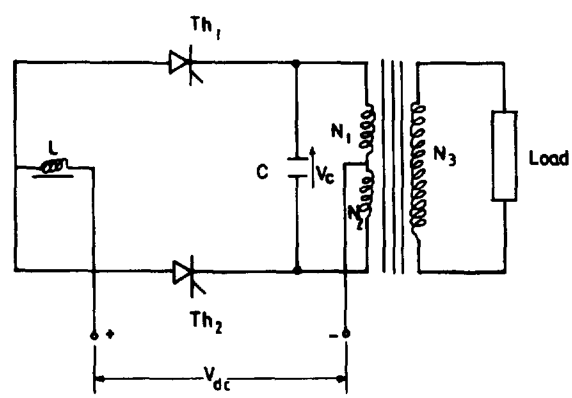

Fig. 1. Thyristor inverter circuit: (*C*) commutating capacitor; (*L*) series inductor; (N_1, N_2) number turns of one half centre-tapped primary winding of the transformer; (N_3) number of turns of the secondary winding; (Th_1, Th_2) thyristors 1 and 2; (V_c) commutating capacitor voltage, and (V_{dc}) battery voltage.

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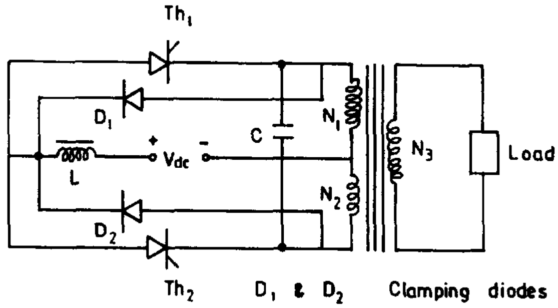

Fig. 2. Thyristor inverter circuit for inductive loads, as in Fig. 1: (D_1, D_2) clamping or free-wheeling diodes.

V_c with a negative polarity towards Th_1 reverse-biases the device, hence turning it 'off'. Therefore, Th_2 conducting the current through N_2 is equal and opposite to the current when Th_1 is conducting.

By applying triggering pulses alternatively to the gates of Th_1 and Th_2, the output voltage waveform at the secondary winding N_3 is an alternating waveform of frequency dependent on the rate at which trigger pulses arrive at the gates of Th_1 and Th_2. The process of switching 'off' the current in the thyristor is called commutation, and the capacitor that applies the reverse voltage V_c to the thyristor is called the commutating capacitor.

For inductive loads, two clamping diodes D_1 and D_2 may be added, see Fig. 2. The diodes provide effective clamping of the voltage in the two halves of the centre-tap transformer in order not to exceed the supply voltage $V_{d.c.}$. (Note, Th_1 and Th_2 are of the same type and same specification and number.)

2.2. Commutating capacitor

The change of the commutating capacitor must be sufficient to maintain the load current for a period equal to or greater than the thyristor's turn-off time.

(i) The charge $Q=It$, where I is the load carried, and t the maximum turn-off time of the thyristor.

(ii) But $Q=CV_c$, where C is the commutating capacitance.

(iii) Hence $CV_c=It$, where V_c is the capacitor voltage, and $C=It/V_c$.

2.3. Series inductance

The series inductance limits the supply current during commutation by keeping the current constant. A smaller commutating capacitor can therefore be used. It also limits the dV/dt as seen by the forward thyristor. The inductance must absorb the energy of the capacitor.

Therefore, $1/2CV_c^2=1/2LI^2$, the inductance $L=CV_c^2/I^2$, but $C=It/V_c$, and $L=V_ct/I$.

The commutating voltage to be used in the calculation of the inductance will be the highest possible capacitor voltage indicating the worst possible condition, giving the inductance value that could cope with the worst case.

2.4. Switching requirement of the thyristors

The dV/dt generated by the switching action of the thyristor is limited by the commutating capacitor and the series inductance.

The maximum dV/dt can be calculated as follows:
if

$$V=V_{max}\sin\omega t$$

and

$$dV/dt=-V_{max}\omega\cos t$$

then dV/dt is maximum when $t=0$
and

$$(dV/dt)_{max}=-V_{max}\omega=-V_{max}2\pi/T$$

and

$$T=2\pi VLC$$

The thyristor selected must have the rate of reapplication of the voltage after commutation within the calculated $(dV/dt)_{max}$ values.

The dI/dt requirement of the thyristor is as important as dV/dt.

$dI/dt)_{max}=-I_{max}2\pi/T$ must be well within the manufacturer's specified values.

For the special case when the circuit is resonant, then

$$\omega L=1/\omega C$$

$$\omega^2=1/LC$$

$$\omega=(LC)^{1/2}$$

$$2f=(LC)^{1/2}$$

where the resonant frequency $f=(LC)^{1/2}/2\pi$.

If dI/dt is chosen, say x A/μs and the thyristor's maximum current is known I_{max}, then

$$T=I_{max}2/(x\ \mathrm{A}/\mu\mathrm{s})$$

and the resonant frequency $f=I/T$ Hz.

2.5. Output transformer design

The UPS operational frequency is 50 Hz, this frequency is the same as the power supply frequency. The estimation of turns' ratio of the transformer is as follows:

$$N_s/N_p\approx\frac{\text{secondary voltage}}{K\times\text{supply voltage}}$$

where N_s is the secondary turns, and N_p the primary turns. K varies from ~1 when the load is resistive to ~1.6 for purely inductive load, normally the average value is used i.e. $K\sim1.3$.

$$N_p=\frac{V10^8}{4AB_{max}fK_1}$$

where V is the primary voltage in one half of the primary winding, A the transformer core area in cm^2, B_{max}, the maximum flux density ~14 500 for many required lamination, and K_1, the winding factor ~0.95.

The total number of turns on the transformer may be traded with the cross-sectional area of the transformer core over a wide range of values with a very little effect on the circuit performance. The more turns are used, the smaller are the core areas required. Large core areas are preferred so that fewer number of turns are needed, thereby making the winding easier. Also large core areas tend to reduce circuit misbehaviour when compared with smaller cores.

2.6. Trigger circuit

The trigger circuit [4,5] provides the signal needed to initiate the conduction of the thyristors. UPSs normally supply power at 50 Hz, the thyristors ought to be fired at that rate. The uni-junction transistor (UJT) trigger circuit is simple and reliable. The basic uni-junction circuit is shown in Fig. 3, and represents a simple timing circuit. The capacitor C charges via the resistance R_T. When the peak point is reached, the capacitor C discharges through the emitter as the UJT switches 'on'. When the emitter voltage V_E reaches 2 V, the UJT ceases to conduct.

The values of R_T and R_{B1} can be calculated so that the cycle is repetitive in order to produce series of pulses as shown.

(i) R_T lies between 3 kΩ and 3 MΩ for contemporary devices, and

(ii) R_{B1} is usually small, < 100 Ω.

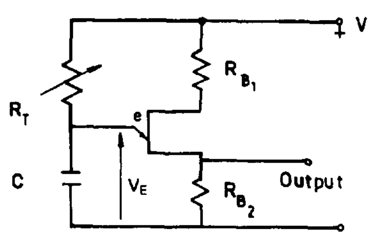

Fig. 3. Uni-junction transistor relaxation oscillator: (C) capacitor; (e) emitter; (R_{B1}) base one resistance; (R_{B2}) base two resistance; (R_T) variable resistance; (V_{BB}) interbase voltage; ($V(_{cc})$ supply voltage, and (V_e) emitter voltage.

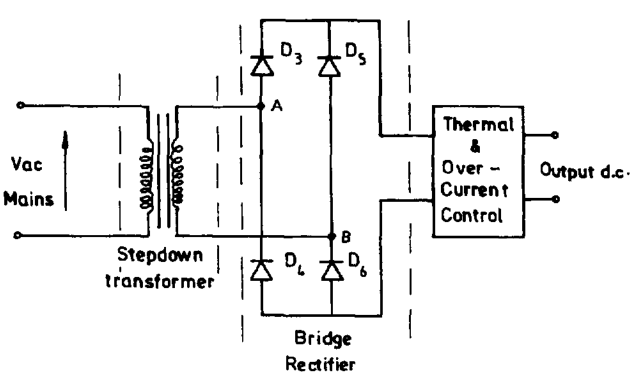

Fig. 4. Battery charger system: (D_3, D_4, D_5, D_6) rectifier diodes, and (V_{ac}) power alternating voltage.

For small values of R_{B1} and R_{B2}, $V_{BB} - V_{cc}$, then the period of the generated signal T is

$$T \sim CR_T \ln(1/(1-\eta))$$

where $\eta = R_{B1}/(R_{B1}-R_{B2}) \sim 0.5$.

The UJT trigger circuit consists of an oscillator, whose output frequency could be varied by the variable resistance R_T.

3. Charger for batteries

12, 24, 36 or 48 V accumulator batteries (usually lead/acid cells) are preferred as the d.c. sources, from which 220–240 V alternating current is generated. A simple step-down transformer in conjunction with a bridge rectifier, see Fig. 4, provides the charging voltage and current. In the bridge-rectifier system, the transformer conducts during both half-cycles of the alternating supply voltage. When the point A is positive with respect to point B, representing the positive half of the cycle, the diodes D_3 and D_6 conduct through the load. During the remaining half-cycle, the point B is positive with respect to point A, and the diodes D_5 and D_4 conduct through the load in the same direction as when point A is positive. For each cycle the above procedure is repeated, producing the rectification of the alternating current supply.

The mean output voltage

$$V_{mean} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, d\omega t$$

$$V_{mean} = \frac{2V_m}{\pi}$$

In general, the bridge rectifier is mounted on heat sinks in order to reduce the working temperature when the diodes are operating at a peak forward current. The charger incorporates both thermal and over-current trip devices to ensure a longer service life.

4. Block diagram of a UPS system

The block diagram is as shown in Fig. 5. The control system operates the change over relays from the power supply

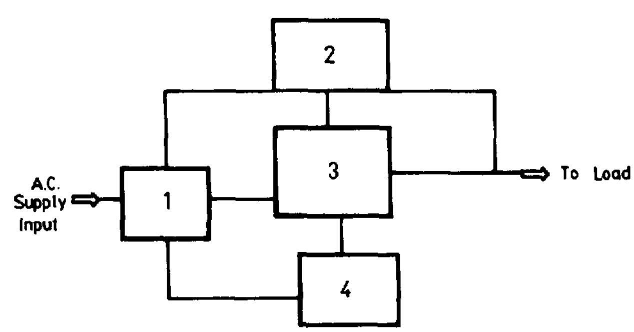

Fig. 5. Block diagram of UPS: (1) control system; (2) protection system; (3) inverter system including trigger circuit and battery, and (4) charger system.

to the inverter output and back again. When the power is 'on', the power is supplied to both the load and the charger system. When the power is 'off', the charger is disconnected as well as the main supply line to the load. The inverter system is energized from the battery. When the power returns, the whole system reverts to the original operating mode.

5. Power rating

Power rating of a UPS is the product of the output voltage and the current. To design a unit, the load voltage and current will determine the rating. The specified values of the voltage and current helps in the selection of correct thyristors and diodes to be used. The overall circuit efficiency should also be considered.

6. Performance evaluation

The inverter, a d.c.–a.c. type, has the conversion efficiency of about 85%. The losses occur as the forward voltage drops in the thyristors and diodes and as losses in the output transformer (these are generated in the cores and in the conductors). The over-current trip for the inverter is incorporated in the control system.

7. Conclusions

An uninterruptible power source (UPS) was designed and built. The system design procedure adopted in this text was successfully used in a computer-aided design programme. As a result, several prototypes were produced. The trigger circuit could use the IC555 timer instead of the uni-junction system mentioned in this paper.

8. List of symbols

A	area of transformer core, cm^2
B_{max}	maximum flux density, wb/m^2
C	commutating capacitor, μF
D_1, D_2	free-wheeling diodes 1 and 2
D_3, D_4, D_5, D_6	rectifier diodes
f	resonant frequency
Hz	hertz
I	load current, A
I_{max}	maximum load current, A
K	winding constant, which varies from 1 to 1.6
K_1	winding factor, ~0.95
L	series inductance
N_1, N_2	number of turns of one half of the centre-tapped primary winding of the transformer
N_3, N_4	number of turns of the secondary winding of the transformer
N_p	number of turns of the primary winding of the transformer
Q	capacitor charge
R_{B1}	base one resistance
R_{B2}	base two resistance
R_T	variable resistance
t	maximum turn-off time of the thyristor
Th_1, Th_2	thyristors 1 and 2
T	period
UJT	uni-junction transistor

Greek letters

$\eta R_{B1}/(R_{B1}+R_{B2})$

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